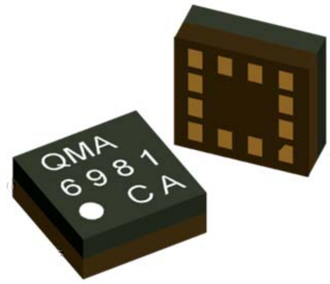
I²C 3-Axis Accelerometer
QMA6981

Advanced Information

The QMA6981 is a single chip three-axis accelerometer. This surface-mount, small sized chip has an integrated acceleration transducer with signal conditioning ASIC, sensing tilt, motion, shock and vibration. It is targeted for applications such as screen rotation, step counting, sleep quality, gaming and personal navigation in mobile and wearable smart devices.



The QMA6981 is based on our state-of-the-art, high resolution single crystal silicon MEMS technology. Along with custom-designed 10-bit ADC ASIC, it offers the advantages of low noise, high accuracy, low power consumption, and offset trimming. The I²C serial bus allows for easy interface.

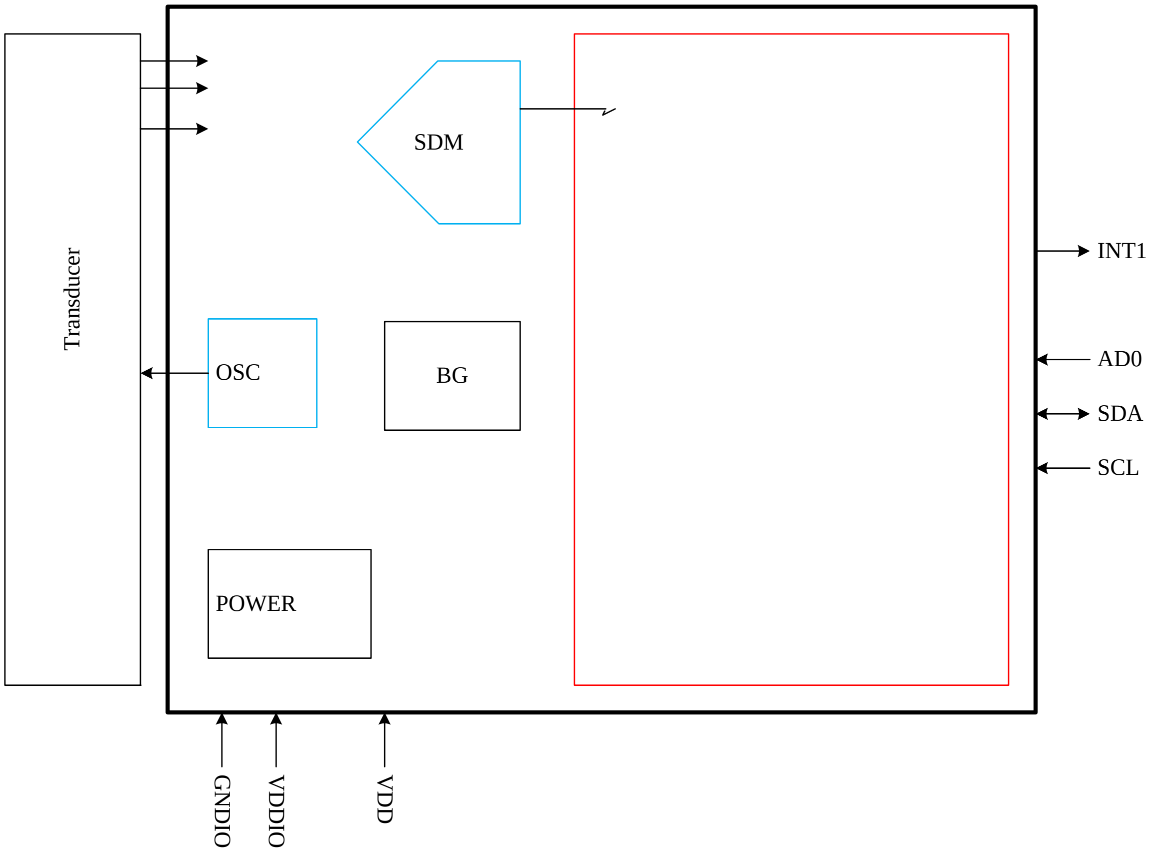
The QMA6981 is in a 2mmx2mmx0.95mm surface mount 12-pin land grid array (LGA) package.

FEATURES	BENEFIT
3-Axis Accelerometer in a 2x2x0.95 mm^3 Land Grid Array Package (LGA), guaranteed to operate over a temperature range of -40 °C to +85 °C.	Small size for highly integrated products. Signals have been digitized and factory trimmed.
10-Bit ADC with low noise accelerometer sensor	High resolution allows for motion and tilt sensing
I^2C Interface with Standard and Fast modes.	High-Speed Interfaces for fast data communications.
Built-In Self-Test	Enables low-cost functionality test after assembly in production
Wide range operation voltage (2.4V To 3.6V) and low power consumption (27-50 µA low power conversion current)	Automatically maintains sensor's sensitivity under wide operation voltage range and compatible with battery powered applications
Integrated FIFO with a depth of 32 frames	High Data-Read rate
RoHS compliant , halogen-free	Environmental protection and wide applications
Built–in motion algorithm	Low power and easy applications including step counting, sleep quality, gaming and personal navigation

CONENTS

1 INTERNAL SCHEMATIC DIAGRAM

1.1 Block Diagram



2 SPECIFICATIONS AND I/O CHARACTERISTICS

2.1 [illegible]

[illegible] 25°C [illegible] 3.0V VDD [illegible]

Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage VDD	VDD, for internal blocks	2.4	3.3	3.6	V
I/O voltage VDDIO	VDDIO, for IO only	1.7		VDD	V
Standby current	VDD and VDDIO on		2		µA
Low power current	BW=500 Hz, ODR=1 Hz		27		µA
Low power current	BW=500 Hz, ODR=10 Hz		29		µA
Low power current	BW=500 Hz, ODR=20 Hz		31		µA
Low power current	BW=500 Hz, ODR=40 Hz		37		µA
Low power current	BW=500 Hz, ODR=100 Hz		50		µA
Full run current	All blocks on, device in run state		220	300	µA
Sleep current	For analog, AFE is off, BG, Transducer and oscillator are on or in low power mode For digital, only counter and FSM are on		55		µA
Deep sleep current	For analog, only BG and oscillator are on For digital, only counter and FSM are on		26		µA
BW	Programmable bandwidth		3.9~500		Hz
Data output rate (ODR)	4*BW (ODRH=1)		15.6~2000		Samples /sec
Conversion time	in full speed		1/(4*BW)		ms

[redacted]

Parameter	Conditions	Min	Typ	Max	Unit
Cross Axis Sensitivity			1		%

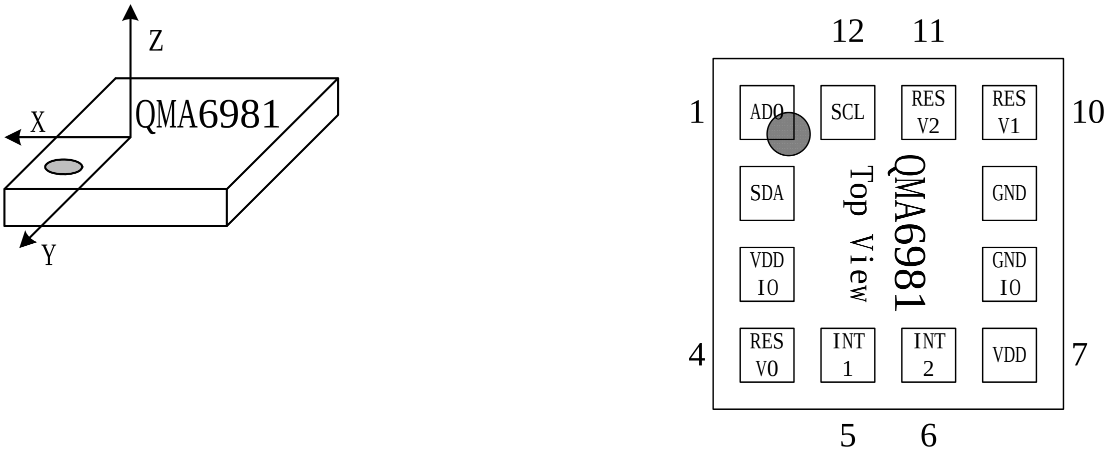


Figure 2. Package View

Table 5. Pin Configuration

PIN No	PIN NAME	I/O	Power Domain	TYPE	Function
1	AD0	I	VDDIO	CMOS	LSB of I^{2}C address
2	SDA	IO	VDDIO	CMOS	Serial data for I^{2}C
3	VDDIO		VDDIO	Power	Power supply to digital interface
4	RESV0	I	VDDIO	CMOS	Reserved. Float or connect to GND
5	INT1	O	VDDIO	CMOS	Interrupt 1
6	INT2	O	VDDIO	CMOS	Interrupt 2
7	VDD		VDD	Power	Power supply to internal block
8	GNDIO		GND	Power	Ground to digital interface
9	GND		GND	Power	Ground to internal block
10	RESV1	IO	VDDIO	CMOS	Reserved
11	RESV2	IO	VDDIO	CMOS	Reserved
12	SCL	I	VDDIO	CMOS	Serial clock for I^{2}C

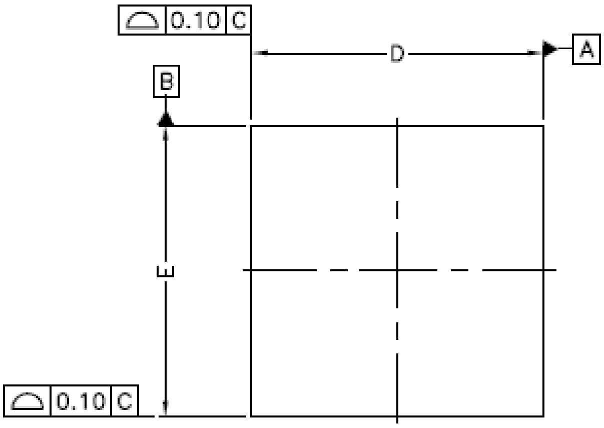
3.2 Package Outline

3.2.1 Package Type

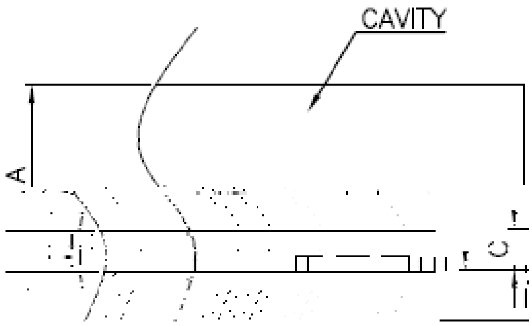
LGA (Land Grid Array)

3.2.2 Package Outline Dimension

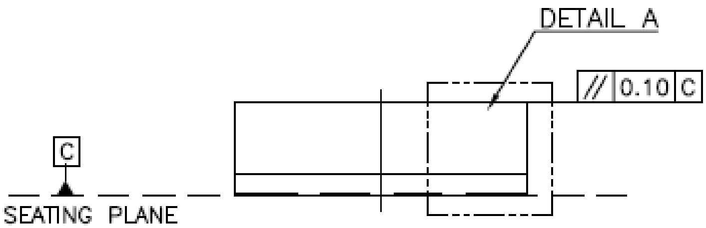
2.0mm (Length)*2.0mm (Width)*0.95mm (Height)



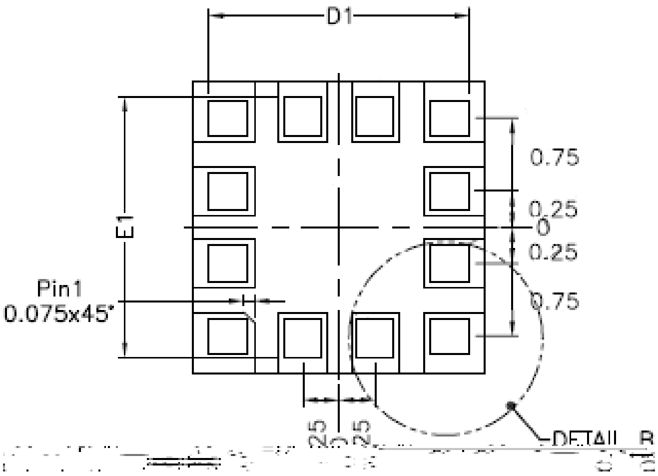
TOP VIEW



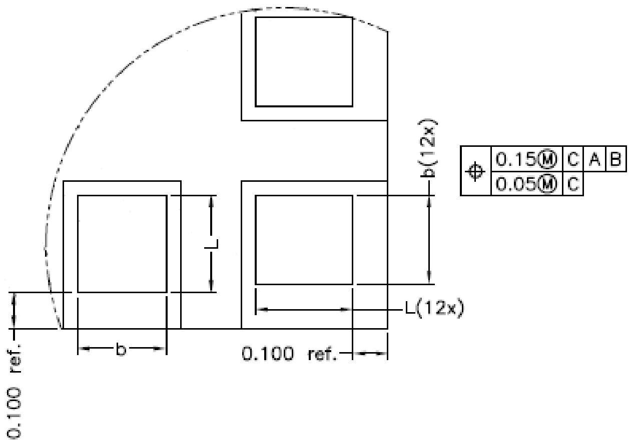
DETAIL A



SIDE VIEW



BOTTOM VIEW



DETAIL B

SYMBOL	DIMENSION (MM)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	0.95	1.00	0.035	0.037	0.039
C	0.16	0.20	0.24	0.006	0.008	0.009
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.95	2.00	2.05	0.077	0.079	0.081
D1	1.80 BSC			0.071 BSC		
E	1.95	2.00	2.05	0.077	0.079	0.081
E1	1.80 BSC			0.071 BSC		
L	0.225	0.275	0.325	0.010	0.012	0.014

Fig3. PgOtDiy

3.2.3 Mg

Fig4. MgFtn

MgF	Dp	Ctn
Line 1	Product Name	“6981” stand for QMA6981
Line 2	Y: the last digital of year CCC: lot code	Lot code: 3 alphanumeric digits, variable to generate mass production trace-code
Line3	P: Part number S: Sub-con ID	P: 1 alphanumeric digit, variable to identify part number S: 1 alphanumeric digit, variable identify sub-con
●	Pin 1 identifier	--

4 EXTERNAL CONNECTION

4.1 [illegible]

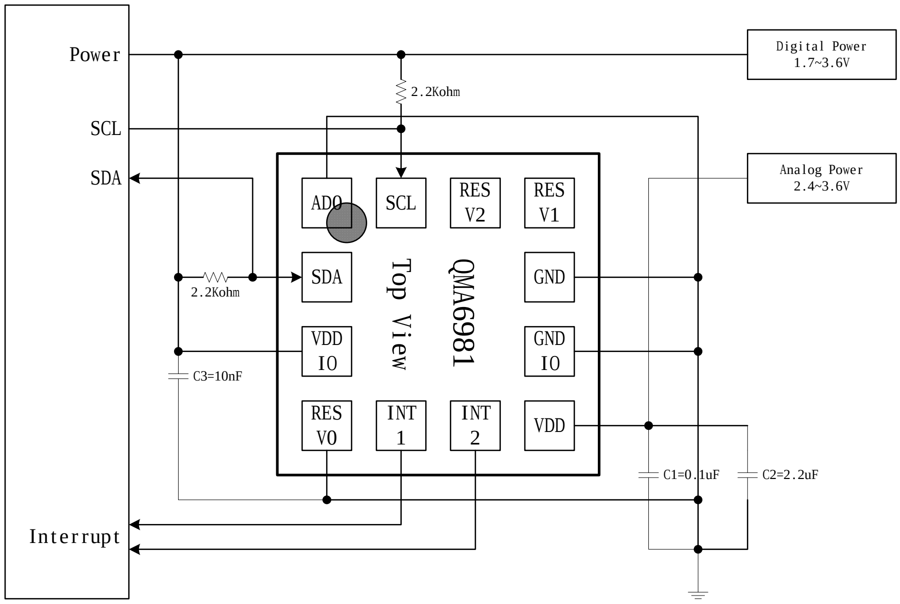


Fig 5. [illegible]

4.2 [illegible]

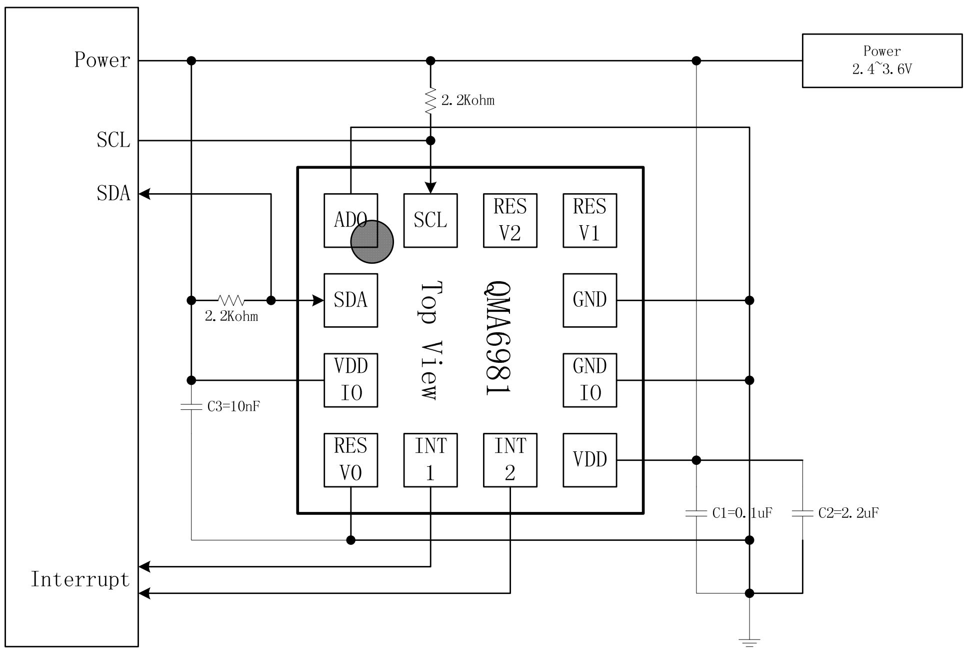


Fig 6. [illegible]

5 BASIC DEVICE OPERATION

5.1 Ates

The QMA6981 acceleration sensor circuit consists of tri-axial sensors and application specific support circuits to measure the acceleration of device. When a DC power supply is applied to the sensor, the sensor converts any accelerating incident in the sensitive axis directions to charge output.

5.2 PwMtgn

Device has two power supply pins. VDD is the main power supply for all of the internal blocks, including analog and digital. VDDIO is a separate power supply, for digital interface only.

The device contains a power-on-reset generator. It generates reset pulse as power on, which can load the register's default value, for the device to function properly.
To make sure the POR block functions well, we should have such constrains on the timing of VDD and VDDIO.

The device should turn-on both power pins in order to operate properly. When the device is powered on, all registers are reset by POR, then the device transits to the standby mode and waits for further commends.

Table 6 provides references for four power states.

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
POR Completion Time	PORT	Time Period After VDD and VDDIO at Operating Voltage to Ready for I^2C Commend and Analogy Measurement.			250	µs
Power off Voltage	SDV	Voltage that Device Considers				

6 MODES OF OPERATION

6.1 Me[illegible]

QMA6981 has two different operational modes, controlled by register (0x11), MODE_BIT. The main purpose of these modes is for power management. The modes can be transited from one to another, as shown below, through I^{2}C commands. The default mode after power-on is standby mode.

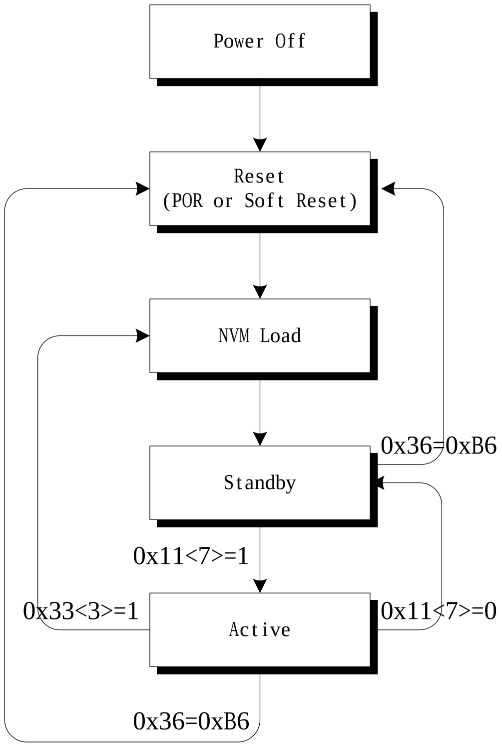


Fig 8. B[illegible]

The default mode after power on is standby mode. Through I^{2}C instruction, device can switch between standby mode and active mode. With SOFTRESET by writing 0xB6 into register 0x36, all of the registers will get default values. SOFTRESET can be done both in active mode and in standby mode. Also, by writing 1 in NVM_LOAD (0x33<3>) when device is in active mode, the NVM related image registers will get default value from NVM, however, other registers will keep the values of their own.

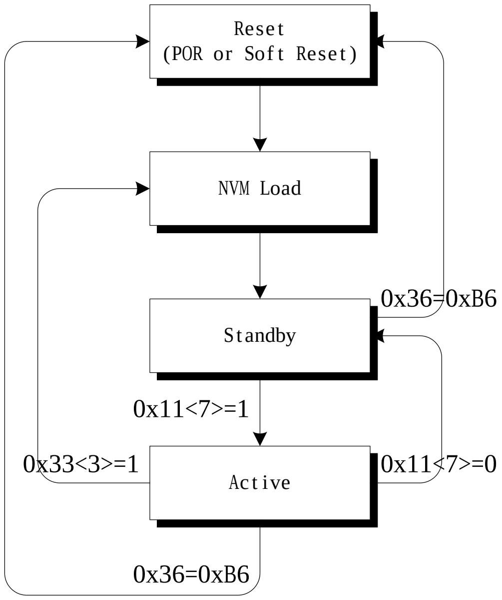


Fig 9. [illegible]

6.2 D[illegible] Modes

6.2.1 Active Mode

In active mode, there are two states, run state, and sleep state.

6.2.1.1 Sleep State

In sleep state, whole signal chain is off, including analog and digital signal conditioning, and the rest blocks are on.

6.2.1.2 Run State

In run state, the ADC digitizes the charge signals from transducer, and digital signal processor conditions these signals in digital domain, processes the interrupts, and send data to FIFO (accessible through register 0x3F) and Data registers (0x01~0x06). After the signal conditioning, the signal chain will be off and device enters back into sleep state, leaves timer and FSM on. Also in sleep state, reference and power blocks are on.

This mode can also be called as power cycling. The power cycling duty is configurable through state registers SLEEP_DUR (0x11<3:0>). Device can enter into active mode by setting MODE_BIT (0x11<7>) to logic 1.
Besides the power cycling, device can also be configured as FULLRUN, by setting SLEEP_DUR=0000b. In this setting, no sleep state in the active mode, and device consumes most power, deliver the data most frequently.

6.2.2 Standby Mode

In standby mode, most of the blocks are off, while device is ready for access through I^2C. Standby mode is the default mode after power on or soft reset. Device can enter into this mode by set the soft reset register (0x36) to 0xB6 or set the MODE_BIT (0x11<7>) to logic 0.
Besides the above two modes, the device also contains NVM loading state. This state is used to reset the value of the NVM related image registers. There are two bits related to this state. When NVM_LOAD (0x33<3>) is set to 1, NVM loading starts. When the device is in NVM loading state, NVM_RDY (0x33<2>) is set to logic 0 by device. After NVM loading is finished, NVM_RDY (0x33<2>) is set back to logic 1 by device, and NVM_LOAD is reset to 0

7 F[illegible]

ASIC support interrupts, such as POL_INT, FOB_INT, STEP_INT, TAP_INT, LOW-G, HIGH-G, DRDY_INT, and FIFO_INT.

7.1 POL_INT

The POL_INT stands for Portrait or Landscape interrupt. It responds to the device in portrait direction or landscape direction. It includes 4 different event types, left, right, up and down events. The different type event stored and can be read from register ORIENT (0x0D<2:0>).

POLA(0x0D<2:0>)	Left	Right	Down	Up	[illegible]
000	0	0	0	0	unknown
001	1	0	0	0	Left/Landscape
010	0	1	0	0	Right/Landscape
101	0	0	1	0	Down/portrait
110	0	0	0	1	Up/portrait

All different events can be detected by comparing the threshold set by register UD_X_TH(0x2D),RL_Y_TH(0x2F) with the sensor data , also have dependency on comparing result between the Z sensor readings and the register UD_Z_TH(0x2C) and RL_Z_TH(0x2E). Hysteresis can be introduced to the angle by decreasing a small offset for the threshold registers. All angle data inside the Hysteresis area will be regarded as unknown status in the orient status register (0x0D<2:0>).

Below Table shows the condition four kinds of orient events generation, the default threshold for X, Y is set to 40 degrees

Event	X	Y	Z
Up	|X|>UD_X_TH X <0		|Z|<UD_Z_TH
Down	|X|>UD_X_TH X >0		|Z|<UD_Z_TH
Right		|Y|>RL_Y_TH Y <0	|Z|<RL_Z_TH
Left		|Y|>RL_Y_TH Y >0	|Z|<RL_Z_TH

For the registers settings, all the orient events threshold 1 LSB bit stand for 3.9mg. For Z axis, it is 8-bit signed 2's complement number ranged from 0.3g to 1.29g, default value 0 as stands for 0.8g. X, Y axis are unsigned data, default value A4 stands for 640mg which angel be regards as 40 degree ,there will be around 10 degree dead band left. The degree value for event can be calculated by the equal asin(0.0039*UD_X_TH) or asin(0.0039*RL_Y_TH).

The related interrupt status bit is ORIENT_INT (0x0A<6>). When the POL status changes the value of ORIENT_INT will be set to logic 1, and this will be cleared after the interrupt status register is read by user. ORIENT_EN (0x16<6>) is the enable bit for the POL_INT. Also, to get this interrupt on PIN_INT1 and/or PIN_INT2, we need to set INT1_ORIENT (0x19<6>) or INT2_ORIENT (0x1B<6>) to logic 1, to map the internal interrupt to the interrupt PINs.

7.2 FOB_INT

The Front/back event can be detected by comparing Z axis data with a low g value, ranged from 0.1g to 0.6g, which is defined by FB_Z_TH(0x30<6:0>). The comparing condition shows below:

Eta	X	Y	Z
Front			|Z|>FB_TH Z>0
Back			|Z|>FB_TH Z<0

The 2 different type events are stored and can be read from register ORIENT (0x0D<4:3>)

FOB(0x0D<4:3>)	ta
00	unknown
01	Front
10	Back
11	Reserved

Angle between the Z-axis and g can have the relationship:
Acc_Z=1g * cos(theta).
Each threshold will introduce a dark area, which the Front/Back status cannot be recognized, the dark area angel is +/- (90-theta).
When the threshold register value is 0x00, the default value stands for 0.1g, and 1 LSB is 3.91mg. The minimum angel between sensor and g direction should be 84 degree, so the dark area should be +/-6 degree. When the value is 0x7F, the dark area should be +/-37 degree.
The related interrupt status bit is FOB_INT (0x0A<7>). When the FOB status changed, the value of FOB_INT will be set to logic 1, and this will be cleared after the interrupt status register is read by user. FOB_EN (0x16<7>) is the enable bit for the FOB_INT. Also, to get this interrupt on PIN_INT1 and/or PIN_INT2, we need to set INT1_FOB (0x19<7>) or INT2_FOB (0x1B<7>) to logic 1, to map the internal interrupt to the interrupt PINs.

7.3 STEP/STEP_QUIT INT

The STEP/STEP_QUIT detect that the user is entering/exiting step mode. When the user enter into step mode, at least one axis sensor data will vary periodically, by numbering the variation periods the step counter can be calculated.

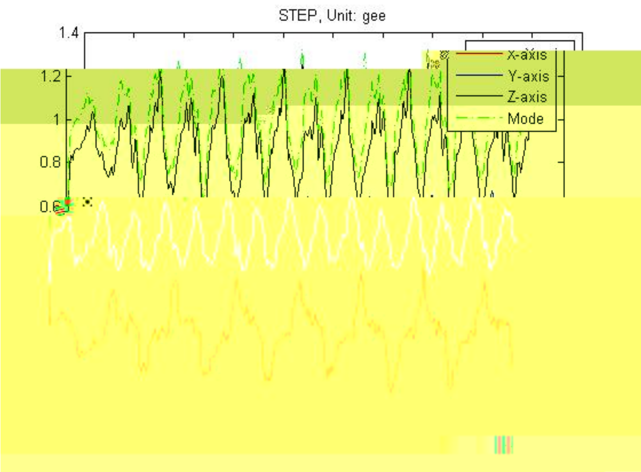


Fig 10. STEP/STEP_Q

Median data (max+min) /2 is called dynamic threshold, the max and min data can be updated by certainly samples, the sample number can be set by register STEP_SAMPLE_CNT (0x12<4:0>). When the sensor data decreasing (or increasing) through the dynamic threshold, a user run step is detected.

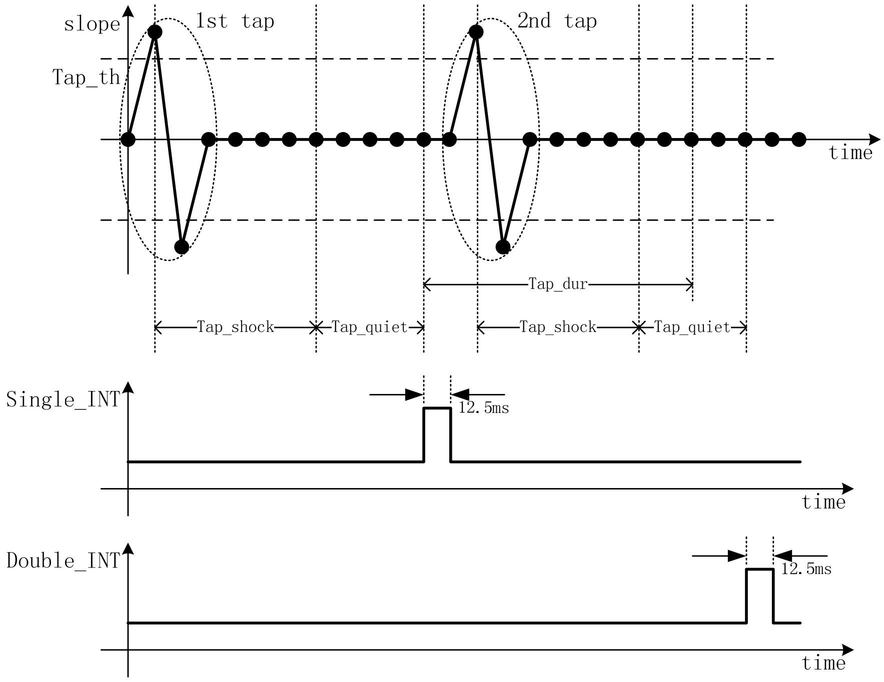


Fig11.

The parameters TAP_SHOCK (0x2A<6>) and TAP_QUIET (0x2A<7>) are affected in both single tap and double tap detection, while TAP_DUR (0x2A<2:0>) is affected in double tap detection only. Within the duration of TAP_SHOCK, any slope exceeding TAP_TH (0x2B<4:0>) after the first event will be ignored. Contrary to this, within duration of TAP_QUIET, no slope exceeding TAP_TH must occur; otherwise the first event will be cancelled.
A single tap interrupt is generated after the combined duration of TAP_SHOCK and TAP_QUIET. The interrupt is cleared after a delay of 12.5ms.
A double tap interrupt is generated if an event fulfilling the conditions for a single tap occurs within the duration defined by TAP_DUR after the completion of the first tap event. The interrupt is cleared after a delay of 12.5ms.
For each of parameter TAP_SHOCK and TAP_QUIET two values are selectable. By writing '0' ('1') to bit TAP_SHOCK, the duration of TAP_SHOCK is set to 50ms (75ms). By writing '0' ('1') to bit TAP_QUIET, the duration of TAP_QUIET is set to 30ms (20ms).
The duration of TAP_DUR can be set by TAP_DUR bits:

TAP_DUR	Duration of TAP_DUR
000	50ms
001	100ms
010	150ms
011	200ms
100	250ms
101	375ms
110	500ms
111	700ms

The axis which triggered the interrupt is indicated by bits TAP_FIRST_X (0x0C<4>), TAP_FIRST_Y (0x0C<5>), and HIGH_FIRST_Z (0x0C<6>). The bit corresponding to the triggering axis contains a '1' while the other bits hold a '0'. These bits hold until new interrupt is triggered.
The sign of the triggering acceleration is stored in bit TAP_SIGN (0x0C<7>). If the (0x0C) HIGH_SIGN = '0' ('1'), the sign is positive (negative). This bit holds until a new interrupt is triggered.

7.5 LOW-G_INT

The low-g interrupt is based on the comparison of acceleration data against a low-g threshold for the detection of free-fall.
The low-g interrupt is enabled (disabled) by writing logic '1' ('0') to bits LOW_EN (0x17<3>). There are two modes available, 'single' mode and 'sum' mode. In 'single' mode, the acceleration of each axis is compared with the threshold; in 'sum' mode, the sum of absolute value of all accelerations │acc_x│+ │acc_y│+│acc_z│ is compared with the threshold. The mode is selected by the contents of the LOW_MODE bit (0x24<2>): '0' means 'single' mode, '1' means 'sum' mode.
The low-g threshold is set through the LOW_TH (0x23<7:0>) register. 1 LSB of LOW_TH always corresponds to an acceleration of 7.8mg (increment is independent from g-range setting).
A hysteresis can be set with the LOW_HYST bits (0x24<1:0>). 1 LSB of LOW_HYST always corresponds to an acceleration of 125mg (as well, increment is independent from g-range setting).
The low-g interrupt is generated if the absolute values of the acceleration of all axes ('and' relation, in case of 'single' mode) or their sum (in case of 'sum' mode) are lower than the threshold for at least the time defined by the LOW_DUR (0x22<7:0>) register. The interrupt is reset if the absolute value of the acceleration of at least one axis ('or' relation, in case of 'single' mode) or the sum of absolute values (in case of 'sum' mode) is higher than the threshold plus the hysteresis for at least one data acquisition. The relation between the content of LOW_DUR and the actual delay of the interrupt generation is delay = [LOW_DUR+1]*2ms. The interrupt status is stored in bit LOW_INT (0x0B<3>).

7.6 HIGH-G_INT

The high-g interrupt is based on the comparison of acceleration data against a high-g threshold for the detection of shock or other high-acceleration events.
The high-g interrupt is enabled (disabled) per axis by writing logic '1' ('0') to bits HIGH_EN_X (0x17<0>), HIGH_EN_Y (0x17<1>), and HIGH_EN_Z (0x17<2>), respectively. The high-g threshold is set through the HIGH_TH (0x26<7:0>) register. The meaning of an LSB of HIGH_TH depends on the selected g-range: it corresponds to 7.8mg in 2g-range (15.6mg in 4g-range, 31.2mg in 8g-range).
A hysteresis can be set with the HIGH_HYST bits (0x24<7:6>). Analogously to the HIGH_TH, the meaning of an LSB of HIGH_HYST depends on the selected g-range: it corresponds to 125mg in 2g-range (250mg in 4g-range, 500mg in 8g-range).
The high-g interrupt is generated if the absolute value of the acceleration data of at least one of the enabled axes ('or' relation) is higher than the threshold for at least the time defined by the HIGH_DUR register (0x25<7:0>). The interrupt is reset if the absolute value of the acceleration of all enabled axes ('and' relation) is lower than the threshold minus the hysteresis. The relation between the content of HIGH_DUR and the actual delay of the interrupt generation is delay = [HIGH_DUR+1]*2ms.
The interrupt status is stored in bit HIGH_INT (0x0B<2>). The axis which triggered the interrupt is indicated by bits HIGH_FIRST_X (0x0C<0>), HIGH_FIRST_Y (0x0C<1>), and HIGH_FIRST_Z (0x0C<2>). The bit corresponding to the triggering axis contains a '1' while the other bits hold a '0'. These bits hold until new interrupt is triggered.
The sign of the triggering acceleration is stored in bit HIGH_SIGN (0x0C<3>). If the (0x0C) HIGH_SIGN = '0' ('1'), the sign is positive (negative). This bit holds until new interrupt is triggered.

7.7 DRDY_INT

The width of the acceleration data is 10 bits, in two's complement representation. The data of each axis is split into 2 parts, the MSB part (one byte contains bit 9 to bit 2) and the LSB part (one byte contains bit 1 to bit 0). Reading data should start with LSB part. When user is reading the LSB byte of data, to ensure the integrity of the acceleration data, the content of MSB can be locked, by setting SHADOW_DIS (0x21<6>) to logic 0. This lock function can be disabled by setting SHADOW_DIS to logic 1. Without lock, the MSB and LSB content will be

Also, the user should note that even with SHADOW_DIS=0, the data of 3 axes are not guaranteed from the same time point. If the user need all of the 3 axes data from the same time point, please use FIFO. For detailed information, the user can refer to 6.8.
If SLEEP_DUR is set to be 0000, then the data can be filtered by low-pass filter, with bandwidth is set by BW (0x10<4:0>). If SLEEP_DUR is set to be other values, the data also can be averaged in different way (set by BW).
In any conditions, the data stored in data registers are offset-compensated.

The device supports four different acceleration measurement ranges. The range is setting through RANGE (0x0F<3:0>), and the details as following:

RANGE	Acceleration range	Resolution
0001	2g	3.9mg/LSB
0010	4g	7.8mg/LSB
0100	8g	15.6mg/LSB
Others	2g	3.9mg/LSB

The interrupt for the new data serves for the synchronous data reading for the host. It is generated after storing a new value of z-axis acceleration data into data register. This interrupt will be cleared automatically when the next data conversion cycle starts, when SLEEP_DUR is not set to 0000b. When device is in full run (SLEEP_DUR=0000), the interrupt will be effective about 128us, and automatically cleared.
The interrupt mode for the new data is fixed to be non-latched.

7.8 FIFOINT

The device has integrated FIFO memory, capable of storing up to 32 frames, with each frame contains three 10 bits words, for acceleration data of x, y, and z axis. All of the 3 axes' acceleration is sampled at same point in time line.

The FIFO can be configured as three modes, FIFO mode, STREAM mode, and BYPASS mode.
FIFO mode.
In FIFO mode, the acceleration data of selected axes are stored in the buffer memory. If enabled, a watermark interrupt can be triggered when the buffer filled up to the defined level. The buffer will continuously be filled until the fill level reaches to 32. When the buffer is full, data collection stops, and the new data will be ignored. Also, FIFO_FULL interrupt will be triggered when enabled.
STREAM mode
In STREAM mode, the acceleration data of selected axes will be stored into the buffer until the buffer is full. The buffer's depth is 31 now. When the buffer is full, data collection continues, and the oldest data is discarded. If enabled, a watermark interrupt will be triggered when the fill level reached to the defined level. Also, when buffer is full, FIFO_FULL interrupt will be triggered if enabled. If any old data is discarded, the FIFO_OR (0x0E<7>) will be set to be logic 1.
BYPASS mode
In BYPASS mode, only the current acceleration data of selected axes can be read out from the FIFO. The FIFO acts like the STREAM mode with a depth of 1. Compare to reading directly from data register, this mode has the advantage of ensuring the package of xyz data are from same point of time line. The data registers are updated sequentially and have chance for the xyz data sampled in different time. Also, if any old data is discarded, the FIFO_OR will be set to be logic 1, similar as that in stream mode.
The FIFO mode can be configured by setting FIFO_MODE (0x3E<7:6>).

FIFO_MODE	Mode
00	BYPASS
01	FIFO
10	STREAM
11	FIFO

User can select the acceleration data of which axes to be stored in the FIFO. This configuration can be done by setting FIFO_CH (0x3E<1:0>), where ‘00b’ for x-, y-, and z-axis, ‘01b’ for x-axis only, ‘10b’ for y-axis only, ‘11b’ for z-axis only.
If all the 3 axes data are selected, the format of data read from 0x3F is as follows

XLSB	XMSB	YLSB	YMSB	ZLSB	ZMSB

These comprise one frame
If only one axis is enabled, the format of data read from 0x3F is as follows

YLSB	YMSB

These comprise one frame
If the frame is not read completely, the remaining parts of the frame will be discarded.
If the FIFO is read beyond the FIFO fill level, all zeroes will be read out.

FIFO_FRAME_COUNTER (0x0E<6:0>) reflects the current fill level of the buffer. If additional data frames are written into the buffer when the FIFO is full (in Stream mode or Bypass mode), then, FIFO_OR (0x0E<7>) is set to 1. This FIFO_OR can be considered as flag of discarding old data.
When a write access to one of the FIFO configuration registers (0x3E) or (0x31) occurs, the FIFO buffer will be cleared, the FIFO fill level indication register FIFO_FRAME_COUNTER (0x0E<6:0>) will be cleared, and the FIFO_OR (0x0E<7>) will be cleared.

As mentioned, FIFO controller contains two interrupts, FIFO_FULL interrupt, and watermark interrupt. These two interrupts are functional in all the FIFO operating modes.
The watermark interrupt is triggered when the fill level of buffer reached to the level that is defined by register FIFO_WM_TRIGGER (0x31<5:0>), if the interrupt is enabled by setting INT_FWM_EN (0x17<6>) to logic 1 and INT1_FWM (0x1A<1>) or INT2_FWM (0x1A<6>) is set.
The FIFO_FULL interrupt is triggered when the buffer has been fully filled. In FIFO-mode [illegible]

In latched mode, the clearings of the interrupt status and selected pin are determined by INT_RD_CLR (0x21<7>). If INT_RD_CLR=0, read operation to the INT_STAT will clear the interrupt and the selected pin. If INT_RD_CLR=1, any read operation to the device will clear the interrupt and the selected pin.
If the condition for trigging the interrupt still holds, the interrupt status will be set again with the next change of the data registers.

Mapping the interrupt pins can be set by INT_MAP (0x19~0x1B).
The electrical interrupt pins can be set in INT_PIN_CONF (0x20<3:0>). The active logic level can be set to 1 or 0, and the interrupt pin can be set to open-drain or push-pull.

If the interrupt mode is configured as latched mode, the interrupt can also be cleared by I^2C reading any of the interrupt status register (0x09 ~ 0x0c).

8 I^{2}C COMMUNICATION PROTOCOL

8.1 I^{2}C Timing

Table 9 and Figure 12 describe the I^{2}C communication protocol times

Table 9. I^{2}C Timing

Parameter	Symbol	Condition	Min

NACK: If the receiver doesn't pull down the SDA line during the high period of the acknowledge clock cycle, it's recognized as NACK by the transmitter.

8.2.3 I^2C W

I^2C write sequence begins with start condition generated by master followed by 7 bits slave address and a write bit (R/W=0). The slave sends an acknowledge bit (ACK=0) and releases the bus. The master sends the one byte register address. The slave again acknowledges the transmission and waits for 8 bits data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

1. I^2C W

START	Slave Address	RW	SACK	Register Address (0x11)	SACK	Data (0x80)	SACK	STOP
	0 0 1 0 0 1 0	0		0 0 0 1 0 0 0 1		1 0 0 0 0 0 0 0		

8.2.4 I^2C R

I^2C write sequence consists of a one-byte I^2C write phase followed by the I^2C read phase. A start condition must be generated between two phase. The I^2C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (R/W=1). Then master releases the bus and waits for the data bytes to be read out from slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACK from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.
The register address is automatically incremented and more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the current I^2C write command.

2. I^2C R

START	Slave Address	RW	SACK	Register Address (0x00)	SACK			
	0 0 1 0 0 1 0	0		0 0 0 0 0 0 0 0				
START	Slave Address	RW	SACK	Data (0x00)	MACK	Data (0x01)		
	0 0 1 0 0 1 0	1		0 0 0 0 0 0 1 0		0 0 0 0 0 0 0 0		
MACK	Data (0x02)		MACK	…………………………………	MACK	Data (0x07)	NACK	STOP
	0 0 0 0 0 0 1 0			…………………………………				

13. Register Map

0x3F		FIFO_DATA<7:0>								R	00
0x3E	FIFO_CONF	FIFO_MODE<1:0>						FIFO_CH<1:0>		RW	00
0x3D		GAIN_Z<7:0>								RW	NVM
0x3C		GAIN_Y<7:0>								RW	NVM
0x3B		GAIN_X<7:0>								RW	NVM
0x3A		OFFSET_Z<7:0>								RW	NVM
0x39		OFFSET_Y<7:0>								RW	NVM
0x38		OFFSET_X<7:0>								RW	NVM
0x37	IMAGE	OFFSET_X<10:8>			GAIN_Z<9:8>		OFFSET_Y<10:8>			RW	NVM
0x36	SOFT_RESET	SOFTRESET: 0xB6								RW	00
0x35										RW	00
0x34										RW	00
0x33	NVM_CFG					NVM_LOAD	NVM_RDY	NVM_PROG		RW	04
0x32	SelfTest	SELFTEST_BIT				SingleEn_Step	SELFTEST_SIGN	SELFTEST_AXIS<1:0>		RW	00
0x31	FIFO_WM			FIFO_WTMK_LVL<5:0>						RW	00
0x30		ORIENT_DB_DI	FB_Z_TH<6:0>							RW	00
0x2F		RL_Y_TH<7:0>								RW	A4
0x2E		RL_Z_TH<7:0>								RW	00
0x2D		UD_X_TH<7:0>								RW	A4
0x2C	4D/6D	UD_Z_TH<7:0>								RW	00
0x2B					TAP_TH<4:0>					RW	0A
0x2A	TAP	TAP_QUIET	TAP_SHOCK				TAP_DUR<2:0>			RW	04
0x29		OS_CUST_Z<7:0>								RW	00
0x28		OS_CUST_Y<7:0>								RW	00
0x27	OS_CUST	OS_CUST_X<7:0>								RW	00
0x26		HIGH_TH<7:0>								RW	C0
0x25		HIGH_DUR<7:0>								RW	0F
0x24		HIGH_HYST<1:0>					LOW_MODE	LOW_HYST<1:0>		RW	81
0x23		LOW_TH<7:0>								RW	30
0x22	LowG_HighG	LOW_DUR<7:0>								RW	09
0x21	INT_LATCH	INT_RD_CLR	SHADOW_DIS	INT_PULSE					LATCH_INT	RW	00
0x20	INT_PIN_CONF					INT2_OD	INT2_LVL	INT1_OD	INT1_LVL	RW	05
0x1F		PEAK_B<5:0>						STEP_MISMATCH_B<1:0>		RW	00
0x1E		VALLEY_B<5:0>								RW	00
0x1D										RW	FF
0x1C			INT2_FWM	INT2_FFULL	INT2_DATA	INT2_LOW	INT2_HIGH			RW	00
0x1B		INT2_FOB	INT2_ORIENT	INT2_S_TAP	INT2_D_TAP	INT2_STEP	INT2_STEP_QUIT	INT2_STEP_UNSIMIL		RW	00
0x1A			INT1_FWM	INT1_FFULL	INT1_DATA	INT1_LOW	INT1_HIGH			RW	00
0x19	INT_MAP	INT1_FOB	INT1_ORIENT	INT1_S_TAP	INT1_D_TAP	INT1_STEP	INT1_STEP_QUIT	INT1_STEP_UNSIMIL		RW	00
0x18	INT_SRC		INT_SRC_STEP	INT_SRC_DATA	INT_SRC_TAP					RW	00
0x17			INT_FWM_EN	INT_FFULL_EN	DATA_EN	LOW_EN	HIGH_EN_Z	HIGH_EN_Y	HIGH_EN_X	RW	00
0x16	INT_EN	FOB_EN	ORIENT_EN	S_TAP_EN	D_TAP_EN	STEP_EN	STEP_QUIT_EN	STEP_UNSIMILAR_EN		RW	00
0x15		STEP_TIME_UP<7:0>								RW	00
0x14		STEP_TIME_LOW<7:0>								RW	00
0x13	STEP_CONF	STEP_CLR	STEP_PRECISION<6:0>							RW	00
0x12		STEP_START			STEP_SAMPLE_COUNT<4:0>					RW	0C
0x11	POWER_MODE	MODE_BIT	RESV	PRESET<1:0>		SLEEP_DUR<3:0>				RW	00
0x10	BW			ODRH	BW<4:0>					RW	00
0x0F	FULL_SCALE					RANGE<3:0>				RW	00
0x0E	FIFO_STATUS	FIFO_OR	FIFO_FRAME_COUNTER<6:0>							R	00
0x0D		STEP_CNT_OVFL			FOB<1:0>		ORIENT<2:0>			R	00
0x0C		TAP_SIGN	TAP_FIRST_Z	TAP_FIRST_Y	TAP_FIRST_X	HIGH_SIGN	HIGH_FIRST_Z	HIGH_FIRST_Y	HIGH_FIRST_X	R	00
0x0B			FIFO_WM_INT	FIFO_FULL_INT	DATA_INT	LOW_INT	HIGH_INT			R	00
0x0A	INT_STATUS	FOB_INT	ORIENT_INT	S_TAP_INT	D_TAP_INT	STEP_INT	STEP_QUIT_INT	STEP_UNSIMILAR		R	00
0x09										R	FF
0x08		STEP_CNT<15:8>								R	00
0x07	STEP_CNT	STEP_CNT<7:0>								R	00
0x06		ACC_Z<9:2>								R	00
0x05		ACC_Z<1:0>							NEW_DATA_Z	R	00
0x04		ACC_Y<9:2>								R	00
0x03		ACC_Y<1:0>							NEW_DATA_Y	R	00
0x02		ACC_X<9:2>								R	00
0x01	DATA	ACC_X<1:0>							NEW_DATA_X	R	00
0x00	CHIP ID	CHIP ID to indicate the product version								RW	BX

9.2 [illegible]

Register 0x00 (CHIP ID)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
Device ID								RW	0xBX

This register is used to identify the device

Register 0x01 ~ 0x02 (DXL, DXM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default

FIFO_WM_INT: 1, FIFO watermark interrupt active
0, FIFO watermark interrupt inactive
FIFO_FULL_INT: 1, FIFO full interrupt active
0, FIFO full interrupt inactive
DATA_INT: 1, data ready interrupt active
0, data ready interrupt inactive
LOW_INT: 1, low-g interrupt active
0, low-g interrupt inactive
HIGH_INT: 1, high-g interrupt active
0, high-g interrupt inactive

Register 0x0c (INT_STAT2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
TAP_SIGN	TAP_FIRST_Z	TAP_FIRST_Y	TAP_FIRST_X	HIGH_SIGN	HIGH_FIRST_Z	HIGH_FIRST_Y	HIGH_FIRST_X	R	0x00

TAP_SIGN: 1, sign of tap triggering is negative
0, sign of tap triggering signal is positive
TAP_FIRST_Z: 1, tap interrupt is triggered by Z axis
0, tap interrupt is not triggered by Z axis
TAP_FIRST_Y: 1, tap interrupt is triggered by Y axis
0, tap interrupt is not triggered by Y axis
TAP_FIRST_X: 1, tap interrupt is triggered by X axis
0, tap interrupt is not triggered by X axis
HIGH_SIGN: 1, sign of high-g triggering signal is negative
0, sign of high-g triggering signal is positive
HIGH_FIRST_Z: 1, high-g interrupt is triggered by Z axis
0, high-g interrupt is not triggered by Z axis
HIGH_FIRST_Y: 1, high-g interrupt is triggered by Y axis
0, high-g interrupt is not triggered by Y axis
HIGH_FIRST_X: 1, high-g interrupt is triggered by X axis
0, high-g interrupt is not triggered by X axis

Register 0x0d (INT_STAT3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CNT_OVFL			FOB<1:0>		ORIENT<2:0>			R	0x00

STEP_CNT_OVFL: 1, step counter is over-flowed
0, step counter is not over-flowed

FOB<1:0>: 00, device is in unknown orientation
01, device is in front orientation
10, device is in back orientation
11, reserved
ORIENT<2:0>: 000, device is in unknown orientation
001, device is in left orientation
010, device is in right orientation
011, reserved
100, reserved
101, device is in down orientation
110, device is in up orientation
111, reserved

Register 0x0e (FIFO_STATE)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_OR	FIFO_FRAME_COUNT<6:0>							R	0x00

FIFO_OR: 1, FIFO over run occurred
0, FIFO over run not occurred
FIFO_FRAME_COUNT<6:0>:
Fill level of FIFO buffer. An empty FIFO corresponds to 0x00. The frame counter can be cleared by reading out all of the frames, or by writing register 0x3e (FIFO_CFG1) or 0x31.

Register 0x0f (RANGE)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
				RANGE<3:0>				RW	0x00

RANGE<3:0>: set the full scale of the accelerometer. Setting as following

Register 0x10 (BW)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
		ODRH	BW<4:0>					RW	0x00

ODRH: 1, higher output data rate, ODR = 4*F_BW
0, lower output data rate, ODR = 2*F_BW

BW<4:0>: bandwidth setting, as following

Register 0x11 (POWER)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
MODE_BIT	RESV	PRESET<1:0>		SLEEP_DUR<3:0>				RW	0x00

MODE_BIT: 1, set device into active mode
0, set device into standby mode

RESV: User should set this bit to 1.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT1_FOB	INT1_ORIENT	INT1_S_TAP	INT1_D_TAP	INT1_STEP	INT1_STEP_QUIT	INT1_STEP_UNSIMILAR		RW	0x00

INT1_FOB: 1, map FOB interrupt to INT1 pin
0, not map FOB interrupt to INT1 pin
INT1_ORIENT: 1, map ORIENT interrupt to INT1 pin
0, not map ORIENT interrupt to INT1 pin
INT1_S_TAP: 1, map single tap interrupt to INT1 pin
0, not map single tap interrupt to INT1 pin
INT1_D_TAP: 1, map double tap interrupt to INT1 pin
0, not map double tap interrupt to INT1 pin
INT1_STEP: 1, map step valid interrupt to INT1 pin
0, not map step valid interrupt to INT1 pin
INT1_STEP_QUIT: 1, map step quit interrupt to INT1 pin
0, not map step quit interrupt to INT1 pin
INT1_STEP_UNSIMILAR:
1, map step unsimilar interrupt to INT1 pin
0, not map step unsimilar interrupt to INT1 pin

Register 0x1a (INT_MAP1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT1_FWM	INT1_FFULL	INT1_DATA	INT1_LOW	INT1_HIGHs			RW	0x00

INT1_FWM: 1, map FIFO watermark interrupt to INT1 pin
0, not map FIFO watermark interrupt to INT1 pin
INT1_FFULL: 1, map FIFO full interrupt to INT1 pin
0, not map FIFO full interrupt to INT1 pin
INT1_DATA: 1, map data ready interrupt to INT1 pin
0, not map data ready interrupt to INT1 pin
INT1_LOW: 1, map low-g interrupt to INT1 pin
0, not map low-g interrupt to INT1 pin
INT1_HIGH: 1, map high-g interrupt to INT1 pin
0, not map high-g interrupt to INT1 pin

Register 0x1B (INT_MAP2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT2_FOB	INT2_ORIENT	INT2_S_TAP	INT2_D_TAP	INT2_STEP	INT2_STEP_QUIT	INT2_STEP_UNSIMILAR		RW	0x00

INT2_FOB: 1, map FOB interrupt to INT2 pin
0, not map FOB interrupt to INT2 pin
INT2_ORIENT: 1, map ORIENT interrupt to INT2 pin
0, not map ORIENT interrupt to INT2 pin
INT2_S_TAP: 1, map single tap interrupt to INT2 pin
0, not map single tap interrupt to INT2 pin
INT2_D_TAP: 1, map double tap interrupt to INT2 pin
0, not map double tap interrupt to INT2 pin
INT2_STEP: 1, map step valid interrupt to INT2 pin
0, not map step valid interrupt to INT2 pin
INT2_STEP_QUIT: 1, map step quit interrupt to INT2 pin
0, not map step quit interrupt to INT2 pin
INT2_STEP_UNSIMILAR:
1, map step unsimilar interrupt to INT2 pin
0, not map step unsimilar interrupt to INT2 pin

Register 0x1c (INT_MAP3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT2_FWM	INT2_FULL	INT2_DATA	INT1_STEP	INT2_LOW	INT2_HIGH		RW	0x00

INT2_FWM: 1, map FIFO watermark interrupt to INT2 pin
0, not map FIFO watermark interrupt to INT2 pin
INT2_FULL: 1, map FIFO full interrupt to INT2 pin
0, not map FIFO full interrupt to INT2 pin
INT2_DATA: 1, map data ready interrupt to INT2 pin
0, not map data ready interrupt to INT2 pin
INT2_LOW: 1, map low-g interrupt to INT2 pin

	0, not map low-g interrupt to INT2 pin
INT2_HIGH:	1, map high-g interrupt to INT2 pin
	0, not map high-g interrupt to INT2 pin

Register 0x20 (INTPIN_CFG)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
				INT2_OD	INT2_LVL	INT1_OD	INT1_LVL	RW	0x05

INT2_OD:	1, open-drain for INT2 pin 0, push-pull for INT2 pin
INT2_LVL:	1, logic high as active level for INT2 pin 0, logic low as active level for INT2 pin
INT1_OD:	1, open-drain for INT1 pin 0, push-pull for INT1 pin
INT1_LVL:	1, logic high as active level for INT1 pin 0, logic low as active level for INT1 pin

Register 0x21 (INT_CFG)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT_RD_CLR	SHADOW_DIS	INT_PULSE					LATCH_INT	RW	0x00

INT_RD_CLR:	1, clear all the interrupts in latched-mode, when any read operation to this device 0, clear all the interrupts, only when read the register INT_STAT (0x0A~0x0B), no matter the interrupts in latched-mode, or in non-latched-mode
SHADOW_DIS:	1, disable the shadowing function for the acceleration data 0, enable the shadowing function for the acceleration data. When shadowing is enabled, the MSB of the acceleration data is locked, when corresponding LSB of the data is reading. This can ensure the integrity of the acceleration data during the reading. The MSB will be unlocked when the MSB is read.
INT_PULSE:	1, data ready interrupt is kept until next conversion starts, in power cycling 0, pulse of data ready interrupt is fixed to be 128us
LATCH_INT:	1, interrupt is in latch mode 0, interrupt is in non-latch mode

Register 0x22 (LOW_HIGH_G_0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
LOW_DUR<7:0>								RW	0x09

LOW_DUR<7:0>: low-g interrupt triggered delay, the actual time is (LOW_DUR<7:0>+1)*2ms; the default delay time is 20ms

Register 0x23 (LOW_HIGH_G_1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
LOW_TH<7:0>								RW	0x30

LOW_TH<7:0>: low-g interrupt threshold, the actual g value is (LOW_TH<7:0>)*7.8mg; the default value is 375mg

Register 0x24 (LOW_HIGH_G_2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
HIGH_HYST<1:0>					LOW_MODE	LOW_HYST<1:0>		RW	0x81

HIGH_HYST<1:0>:	hysteresis of high-g interrupt , the actual g value is (HIGH_HYST<1:0>)*125mg(2g range), (HIGH_HYST<1:0>)*250mg (4g range),(HIGH_HYST<1:0>)*500mg(8g range)
LOW_MODE:	low-g interrupt mode 1: sum mode 0: single-axis mode,
LOW_HYST<1:0>:	hysteresis of low-g interrupt , the actual g value is (LOW_HYST<1:0>)*125mg, independent of the selected g range

Register 0x25 (LOW_HIGH_G_3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
HIGH_DUR<7:0>								RW	0x0F

HIGH_DUR<7:0>: high-g interrupt triggered delay, the actual time is (HIGH_DUR<7:0>+1)*2ms; the default delay time is 32ms

Register 0x26 (LOW_HIGH_G_4)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
HIGH_TH<7:0>								RW	0xC0

HIGH_TH<7:0>: high-g interrupt threshold, the actual g value is (HIGH_TH<7:0>)*7.8mg(2g range), (HIGH_TH<7:0>)*15.6mg(4g range), (HIGH_TH<7:0>)*31.2mg(8g range)

Register 0x27 (OS_CUST_X)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_X<7:0>								RW	0x00

OS_CUST_X<7:0>: offset calibration of X axis for user, the LSB depends on full-scale of the device which is 3.9mg in 2g range, 7.8mg in 4g range, 15.6mg in 8g range

Register 0x28 (OS_CUST_Y)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_Y<7:0>								RW	0x00

OS_CUST_Y<7:0>: offset calibration of Y axis for user, the LSB depends on full-scale of the device which is 3.9mg in 2g range, 7.8mg in 4g range, 15.6mg in 8g range

Register 0x29 (OS_CUST_Z)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_Z<7:0>								RW	0x00

OS_CUST_Z<7:0>: offset calibration of Z axis for user, the LSB depends on full-scale of the device which is 3.9mg in 2g range, 7.8mg in 4g range, 15.6mg in 8g range

Register 0x2a (TAP_CONF0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
TAP_QUIET	TAP_SHOCK				TAP_DUR<2:0>			RW	0x04

TAP_QUIET: tap quiet time, 1: 30ms, 0: 20ms
TAP_SHOCK: tap shock time, 1: 50ms, 0: 75ms
TAP_DUR<2:0>: the time window of the second tap event for double tap

TAP_DUR<2:0>	Duration of TAP_DUR
000	50ms
001	100ms
010	150ms
011	200ms
100	250ms
101	375ms
110	500ms
111	700ms

Register 0x2b (TAP_CONF1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
			TAP_TH<4:0>					RW	0x00

TAP_TH<4:0>: threshold of single/double tap interrupt, the actual g value is TAP_TH<4:0>*62.5mg (2g range), TAP_TH<4:0>*125mg(4g range), TAP_TH<4:0>*250mg(8g range)

Register 0x2c (4D6D_CONF0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
UD_Z_TH<7:0>								RW	0x00

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_MODE<1:0>						FIFO_CH<1:0>		RW	0x00

FIFO_MODE<1:0>: FIFO_MODE defines FIFO mode of the device. Settings as following

FIFO_MODE<1:0>	Mode

FIFO_CH<1:0>: FIFO_CH defines which channel data be stored in FIFO buffer. Setting as following
11, only z axis data be stored in FIFO buffer
10, only y axis data be stored in FIFO buffer
01, only x axis data be stored in FIFO buffer
00, all axes data be stored in FIFO buffer

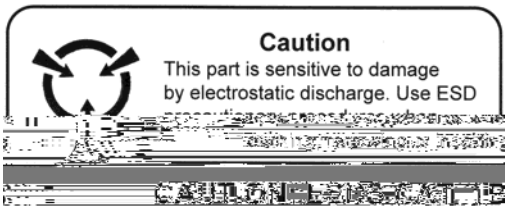
Register 0x3f (FIFO_DATA)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_DATA								R	0x00

FIFO_DATA: FIFO read out data. User can read out FIFO data through this register. Data format depends on the setting of FIFO_CH (0x3e<1:0>).
When the FIFO data is the LSB part of acceleration data, and if FIFO is empty, then FIFO_DATA<0> is 0. Otherwise if FIFO is not empty and the data is effective, FIFO_DATA<0> is 1 when reading LSB of acceleration.

ORDERING INFORMATION

OigNbn	TR	Pkg	Pkg
QMA6981-TR	-40 ~85	LGA-12	Tape and Reel: 5k pieces/reel



FIND OUMOR

For more information on QST's Accelerometer Sensors contact us at 86-21-50497300.

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ISO9001 : 2008

China Patents 201510000399.8, 201510000425.7, 201310426346.3, 201310426677.7, 201310426729.0, 201210585811.3 and 201210553014.7 apply to the technology described.

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